Power-constrained Era: Logic Technology Implications

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Outline

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- Power Constrain – Logic Technology Implications
- Technology Architecture Outlook
  - Steep Sub-threshold devices
  - High-mobility channels
  - Interconnect R/C
- Other routes to overcome power constrains
  - 3D-IC and system integration
- Summary

Summary

- Circuit density will continue to increase ~2x/node
- New logic technologies expected to maintain constant power density will still achieving > 1x speed improvement / node
- Semiconductor technology scaling poses a wealth of technical challenges and thus opportunities for innovation – transistor and interconnect architectures, design, packaging, and system integration
- Leakage and active power drive the need for structural and material changes in advanced logic technologies
- Significant steps towards low V_{DD} operation have been made with high-mobility channel devices – performance still a critical challenge
- Energy efficiency through 3D-IC and system-level integration is also key enabler for continued performance per watt improvement